SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : FPGA ARCHITECTURE & APPLICATIONS (16EC5708)

Branch& Specialization: ECE-ES&VLSI **Year & Sem:** M.TECH-II SEM

UNIT-I
PROGRAMMABLE LOGIC

1.(a) Design a PLA circuit for the following function [5M]
(b) Explain the LAB of Altera max 7000 CPLD with a neat structural diagram [5M]
2 (a) Draw the structure of PAL and explain it. [5M]
. (b) Draw the logic diagram of MAX 7000 CPLD microcell and explain its functioning [5M]
3. (a) Design the following function using ROMs. [5M]

$F=XYZ^{I}+Y^{I}Z+X\,{}^{I}Y^{I}$

(b)Compare the salient features of AMD's CPLD Mach 1 to 5. [5M]
4.(a) Discuss about speed performance and in-system programmability of lattice PLST's architecture in 3000 series. [5M]
(b) Compare PLA, PAL and PLDs with respect to different features, programming and Applications. . [5M]
5. (a) Explain in detail about FPGA based system design [5M]
(b) What are the various methodologies of FPGA? Explain the same with neat diagram [5M]
6.(a) Give the functional description of the Altera's MAX 7000 PLD with the help of logical array block and Macro cell Diagrams [5M]
(b) Explain the LAB of Altera FLEX Logic 10000 series CPLD with a neat structural diagram [5M]
7. (a) Compare the salient features of AMD's CPLD Mach 1 to 5. [5M]
(b) Implement the following Boolean function using PAL: [5M]
$F(w, x, y, z) = \Sigma m\,(0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$
8.(a) Distinguish between FPGA and CPLD. [5M]
(b) Draw the structure of PLA and explain it. [5M]
9.(a). Draw the structure of PAL and explain it. [5M]
(b). Draw the structure of SRAM controlled programmable switches and explain its function. [5M]
10. (a) Explain the feature of Cypress FLASH 370 device technology. [5M]
(b).Design a PLA circuit for the following function [5M]
$F=ab^{1}c+a^{1}c^{1}+ba^{1}$

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UNIT-II
FPGA AND CASE STUDIES

1.(a) Explain the architecture and speed performance of Actel's ACT2 FPGA family. [5M]

(b)Impliment the 8 to1 multiplexer using FLEX10000 device. How many logic elements Are required? [5M]

2.(a)Explain about the state assignment for FPGA. [5M]

(b)Give the basic properties of petrinet Explain the traffic light controller design using Petrinet notation. [5M]

3. (a)realize switching function(2,3,4,6,7)using 2 input LUTS.Give the truth table implementation In each LUT swow wires in FPGA. [5M]

(b)Explain about the state assignment for FPGA. [5M]

4. (a) Explain the application of the Hot method to a serial 2's complement. [5M]

(b).Give the basic properties of petrinet Explain the traffic light controller design using Petrinet notation. [5M]

5. (a) Write about FPGA and compare the speed performance of ACT1,ACT2,ACT3 FPGA.[5]

(b)Draw the explain the architecture of optimized reconfigurable cell array of AT&T. [5M]

6. (a) Draw the architecture of Altera flex 8000 FPGAs and Explain it. [5M]

(b)compare the speed performance of ACT 1,2,3. [5M]

7. (a) Explain the functions of different blocks in Xilinx XC4000 CLB.[5M]

(b)What is LE?Draw and Explain the working of LE of Alteral FLEX 8000. [5M]

8. (a) Explain about the state assignment for FPGA. [5M]

9. Explain about XC4000 AND ALTERA.s FLEX 8000. [5M]

10.(a) Draw and explain logic blocks of FPGAs. [5M]

(b)Explain the design flow of FPGAs. [5M]

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UNIT-III

FINITE STATE MECHINES(FSM)

1.(a) What is FSM?How it is used for FPGA [5M]

(b)How one hot state machine differs from other encoded state machines [5M]

2.(a) What is state transistion table?Explain how state assignment can be carried for FPGA [5M]

(b) Explain the procedure for design a state machine using one hot encoding [5M]

3.(a)Explain about symbolic representation of FSM architectures and how it is different from ASM.[5M]

(b)Discuss the problem of intial state assignment for one hot encoding and explain the procedure to design a state machine [5M]

4. (a) Explain the basic concepts of petrinets and state its properities [5M]

(b).discuss (i) metastability (ii) synchronization [5M]

5.(a) Explain Derivations of state machine charges [5M]

(b) Write about linked state machine [5M]

6. (a)Explain about chans with a PAL. [5M]

(b)Explain about Alternative realization for state machine chans using microprograms. [5M]

7.(a)Explain about Linked state macine. [5M]

(b) One Hot state machine. [5M]

8. (a) What is FSM?How it is used for FPGA [5M]

(b) Explain Derivations of state machine charges [5M]

9.(a) Explain Derivations of state machine charges [5M]

(b) Explain the procedure for design a state machine using one hot encoding [5M]

10. Explain about symbolic representation of FSM architectures and how it is different from ASM. [10M]

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UNIT-IV

FSM ARCHITECTURES AND SYSTEM LEVEL DESIGN

1.(a)What are the petri nets? How these are used in the design of state machine? [5M]

(b)Explain the design of extended petri nets for parallel controllers . [5M]

2.Write a short notes on the following. [5M]

(a)Use of ASMs in one –hot design.

(b)Metastability. [5M]

3. (a)Explain how ASMs are used in the design of one-hot state machine. [5M]

(b)Design a data path bus using one –hot method. [5M]

4.Write a short notes on the following.

(a)State machine design centered around shift registers. [5M]

(b)Cypress FLAH 370 device technology. [5M]

5. With an example explain about one-hot design method using ASMs. [10M]

6.(a)Explain about the top down design approaches of a state machine. [5M]

(b)Describe the extended petri nets for parallel controllers. [5M]

7. (a) Describe how state machine charts are realized with PAL. [5M]

(b)Explain for use of ASMs in one-hot design. [5M]

8.(a)State machine design centered around shift registers. [5M]

(b)Explain K application of one –hot method. [5M]

9 .(a) Use of ASMs in one –hot design. [5M]

(b)Explain how ASMs are used in the design of one-hot state machine. [5M]

10. State machine design centered around shift registers. [10M]

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UNIT-V
CASE STUDIES

1. Explain the Combinational Logic circuits. [10M]
2. Explain about the parallel adder cell. [10M]
3. Design a decade counter and explain the process of implementing their design on FPGAs.. [10M]
4. Write short notes on the following:
   (a) Counters and multiplexers. [5M]
   (b)Parallel adder sequential circuits. [5M]
5. (a) Design a BCD counter using appropriate programmable logic elements or device. [5M]
   (b)Write the HDL code for the design of 4-bit parallel adder using four 1-bit parallel adders. [5M]
6. Discuss parallel adder sequential circuit. [10M]
7. Write the HDL code for the design of 4-bit parallel adder using four 1-bit parallel adders. [10M]
8. (a) Discuss a 4 bit parallel adder circuit. [5M]
   (b).Design a parallel adder sequential circuit. [5M]
9. (a).Explain about Decade counters. [5M]
   (b). Discuss a parallel controller design. [5M]
10. (a) Explain decade counters. [5M]
    (b) Multipliers. [5M]
11. (a)Design a 4-bit parallel adder circuit. [5M]
    (b)Design a parallel to serial Adder/subtractor controller. [5M]